IN THE CLAIMS

Please cancel claims 27-29.

Please amend claims 5, 22 and 24-26 as follows:

1. (Original) A method of calibrating a read circuit in a magnetic memory, comprising:

measuring a calibration value;

performing a large error calibration of a magnetic memory cell if the calibration value is within a maximum range;

performing a small error calibration of the magnetic memory cell if the calibration value is within a minimum range;

performing a first read operation on the magnetic memory; and

performing a second read operation on the magnetic memory.

2. (Original) The method of claim 1, further comprising measuring the calibration value after the large error calibration has been performed.

3. (Original) The method of claim 1, further comprising measuring the calibration value after the small error calibration has been performed.

4. (Original) The method of claim 1, the read circuit including an integrator, wherein measuring the calibration value comprises:

measuring an amount of time for a voltage on the integrator to decay to a reference voltage, wherein the calibration value corresponds to the time.

5. (Currently Amended) ~~The method of claim 4~~ A method of calibrating a read circuit in a magnetic memory, comprising:

measuring a calibration value;

performing a large error calibration of a magnetic memory cell if the calibration value is within a maximum range;

performing a small error calibration of the magnetic memory cell if the calibration value is within a minimum range;

performing a first read operation on the magnetic memory;

performing a second read operation on the magnetic memory; and

the read circuit including an integrator, wherein measuring the calibration value comprises:

measuring an amount of time for a voltage on the integrator to decay to a reference voltage, wherein the calibration value corresponds to the time, wherein the maximum range includes a maximum upper threshold value and a maximum lower threshold value, and wherein the large error calibration is performed if the calibration value is greater than the maximum upper threshold value or less than the maximum lower threshold value.

6. (Original) The method of claim 5, wherein the minimum range includes a minimum upper threshold value and a minimum lower threshold value, and wherein the small error calibration is performed if the calibration value is equal to or greater than the maximum lower threshold value and less than the minimum lower threshold value, or is greater than the minimum upper threshold value and equal to or less than the maximum upper threshold value.

7. (Original) The method of claim 1, wherein performing the large error calibration comprises:

performing a coarse calibration of the read circuit; and

performing a fine calibration of the read circuit.

8. (Original) The method of claim 7, the read circuit including a direct injection charge amplifier having at least one transistor in an isolated well, wherein performing the coarse calibration comprises:

generating a test signal;

supplying an input signal to the direct injection charge amplifier;

comparing an output signal of the direct injection charge amplifier to the test signal; and adjusting a back gate bias voltage to the isolated well.

9. (Original) The method of claim 8, wherein performing the fine calibration comprises:

adjusting a transistor impedance; and

storing a number that corresponds to the back gate bias voltage and the transistor impedance that causes the output signal to be within an acceptable limit of the test signal.

10. (Original) The method of claim 1, wherein performing the small error calibration comprises:

performing a fine calibration of the read circuit.

11. (Original) The method of claim 10, the read circuit including a direct injection charge amplifier, wherein performing the fine calibration comprises:

generating a test signal;

supplying an input signal;

comparing an output signal to the test signal;

adjusting a transistor impedance; and

storing a number that corresponds to the transistor impedance that causes the output signal to be within an acceptable limit of the test signal.

12. (Original) A method of calibrating a read circuit in a magnetic memory which includes an array of bit lines extending in a first direction which intersect an array of memory cells and an array of word lines extending in a second direction which intersect the array of memory cells, wherein a number of word lines in the array of word lines is equal to or greater than M, comprising:

selecting, for (i) equal to one, an (i) word line from the array of word lines and one bit line from the array of bit lines which intersect an (i) memory cell from the array of memory cells;

measuring a calibration value;

performing a large error calibration if the calibration value is greater than a maximum upper threshold value or less than a maximum lower threshold value;

performing a small error calibration if the calibration value is equal to or greater than the maximum lower threshold value and less than a minimum lower threshold value, or is greater than a minimum upper threshold value and equal to or less than the maximum upper threshold value; and

performing a read operation on the first memory cell;

for each value of (i) for $2 \leq i \leq M$;

selecting the (i) word line from the array of word lines and the one bit line from the array of bit lines which intersect the (i) memory cell from the array of memory cells; and

performing a read operation on the (i) memory cell.

13. (Original) The method of claim 12, further comprising measuring the calibration value after the large error calibration has been performed.

14. (Original) The method of claim 12, further comprising measuring the calibration value after the small error calibration has been performed.

15. (Original) The method of claim 12, the read circuit including an integrator, wherein measuring the calibration value comprises:

measuring an amount of time for a voltage on the integrator to decay to a reference voltage, wherein the calibration value corresponds to the time.

16. (Original) The method of claim 12, wherein performing the large error calibration comprises:

performing a coarse calibration of the read circuit; and

performing a fine calibration of the read circuit.

17. (Original) The method of claim 16, the read circuit including a direct injection charge amplifier having at least one transistor in an isolated well, wherein performing the coarse calibration comprises:

generating a test signal;

supplying an input signal to the direct injection charge amplifier;

comparing an output signal of the direct injection charge amplifier to the test signal; and

adjusting a back gate bias voltage to the isolated well.

18. (Original) The method of claim 17, wherein performing the fine calibration comprises:

adjusting a transistor impedance; and

storing a number that corresponds to the back gate bias voltage and the transistor impedance that causes the output signal to be within an acceptable limit of the test signal.

19. (Original) The method of claim 12, wherein performing the small error calibration comprises:

performing a fine calibration of the read circuit.

20. (Original) The method of claim 19, the read circuit including a direct injection charge amplifier, wherein performing the fine calibration comprises:

generating a test signal;

supplying an input signal;

comparing an output signal to the test signal;

adjusting a transistor impedance; and

storing a number that corresponds to the transistor impedance that causes the output signal to be within an acceptable limit of the test signal.

21. (Original) The method of claim 12, wherein selecting the (i) word line from the array of word lines and the one bit line from the array of bit lines which intersect the (i) memory cell from the array of memory cells includes:

applying a first potential to the (i) word line from the array of word lines; and

applying a second potential to the one bit line from the array of bit lines, wherein the first potential is a ground potential and the second potential is an array voltage potential.

22. (Currently Amended) A magnetic random access memory comprising:

a magnetic memory cell;

a read circuit for performing a read operation to the memory cell;

a control circuit configured to calibrate the read circuit including measuring a calibration of the magnetic memory cell, and performing a large error calibration if the calibration value is within a maximum range.~~ to perform a small error calibration if the calibration value is within a minimum range.~~

23. (Original) The magnetic memory of claim 22, where the control circuit is configured to perform a small error calibration if the calibration value is within a minimum range.

24. (Currently Amended)~~ The magnetic memory of claim 1~~A magnetic random access memory comprising:

a magnetic memory cell;

a read circuit for performing a read operation to the memory cell;

a control circuit configured to calibrate the read circuit including measuring a calibration of the magnetic memory cell, and performing a large error calibration if the calibration value is within a maximum range, the read circuit comprising an integrator, and where the control circuit is configured to measure the amount of time for a voltage decay on the integrator to decay to a reference voltage, where the calibration value corresponds to the time.

25. (Currently Amended)~~ The memory of claim 22~~A magnetic random access memory comprising:

a magnetic memory cell;

a read circuit for performing a read operation to the memory cell;

a control circuit configured to calibrate the read circuit including measuring a calibration of the magnetic memory cell, and performing a large error calibration if the calibration value is within a maximum range, the read circuit comprising a direct ~~i8njection~~injection charge amplifier having at least one transistor in an isolated well and where the control circuit is configured to perform the coarse calibration by generating a test signal, supplying an input signal to the direct injection charge amplifier, compOaring an output signal of the direct injection charge amplifier to the test signal, and adjusting a back gate bias voltage to the isolated well.

26. (Currently Amended) ~~The memory of claim 22~~A magnetic random access memory comprising:

a magnetic memory cell;

a read circuit for performing a read operation to the memory cell;

a control circuit configured to calibrate the read circuit including measuring a calibration of the magnetic memory cell, and performing a large error calibration if the calibration value is within a maximum range, the read circuit including a direct injection charge amplifier used for performing the fine calibration.

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)